VERIFICATION OF A TRANSLATION

I, the translator Dr. Walter Kufner, hereby declare:

My name and post office address are as stated below.

I am knowledgeable in the English language and in the language in which the below identified application was filed, and that I believe the English translation of PCT/DE 03/03739 (WO 2004/044994) filed on November 12, 2003, is a true and complete translation.

All statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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MONOLITHICALLY INTEGRATED VERTICAL PIN PHOTODIODE IN BICMOS TECHNOLOGY

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The present invention relates to an improved vertical PIN photodiode monolithically integrated in a biCMOS technology and to a method of forming the same.

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Discrete PIN photodiodes having a slightly doped i-zone with a thickness of several 10μm formed in silicon technology represent prior art. With PIN photodiodes monolithically integrated into silicon chips, however, the problem to be solved is that the dopant concentration of the substrate ranges from $10^{15}\,cm^{-3}$ and even higher for CMOS wells and n-collectors / epitaxial layers of npn transistors formed in bipolar and biCMOS technology. For this reason, in non-modified SBC (standard buried collector) technology, processes based on bipolar and biCMOS technology, merely PIN photodiodes are feasible which have a thin i-zone (approximately 1μm in sophisticated processes), thereby resulting in a low efficiency of approximately 26% at 650/670 nm and even less at longer wavelengths (approximately 10% efficiency at 850 nm), as is, for example disclosed by Lim et al., Digest Technical Papers, ISSCC, 1993, pages 696 to 697 and by Kuchta et al., IBM Journal Res. Develop. 39, pages 63 to 72, 1995.

This problem was solved for PIN diodes integrated into bipolar circuitry on silicon substrates by a sophisticated epitaxial process including an intermediate step, which was additionally introduced into the overall process, so as to form a 15 μm thick slightly doped i-zone, cf. Yamamoto et al, IEEE Trans. Electron. Dev. 42(1), pages 58-63, 1995. For this purpose, at least three additional masking steps are necessary, thereby significantly contributing to production costs of the process. Another approach in this respect represent so-called lateral trench PIN photodiodes, cf. Yang et al., IEEE Electron. Dev. Lett., pages 395-397, 2002, this approach, however, requiring additional efforts in the integration scheme.

In the CMOS technology, the PIN photodiode integration is already solved, cf. Zimmermann, IEEE Photonics Technology Letters 11, pages 254-256. Here, the i-zone is realized by a slightly doped n-epitaxial layer deposited on the n^+ substrate. To this end, an additional masking step is necessary.

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It is an object of the present invention and, thus, the problem underlying the present invention is, to enhance a vertical integrated photodiode formed in biCMOS technology with respect to its operating speed and its efficiency without (substantially) increased efforts involved in the manufacturing process.

The present invention provides for an improvement of the data of OEIC (optoelectronic integrated circuits), which are based on the biCMOS technology, thereby allowing an extension of its applications.

According to the present invention, this object is solved by forming the i-zone of the PIN diode (or PIN photodiode) by means of the combination of a p^- epitaxial layer having a thickness up to 15µm and having a low dopant concentration of particularly approximately 10^{13} cm^{-3} (for a thinner p^- epitaxial layer a higher dopant concentration is sufficient), which is located on the highly doped p^+ substrate, with a doped n^- epitxatial layer preferably substantially doped at 10^{14} cm^{-3} that is located adjacent to the former epitaxial layer and into which the n^+ cathode of the PIN photodiode is incorporated, and by laterally bordering the n^- epitaxial layer by p well regions in the lateral direction, and by providing buried p layers located under the p well regions, which extend into the p epitaxial layer.

In addition to the anode terminals via the p wells used for the lateral insulation of the PIN photodiode on the top surface of the chip, an anode contact (as an area or as a contact) is provided on the bottom side of the chip. To this end, at least in this back side anode area, the substrate may be thinned (claim 3.)

The back side contact may be omitted, if the serial resistance of the photodiode having an anode on the planar front surface, which is contacted in a precisely known manner, is not too great (claim 4). For example, deep trench contacts may be formed from the top so as to reduce the serial resistance (claim 5).

For a deeper understanding as to how such a photodiode structure requiring minimum additional technological efforts may be realized in biCMOS technology, the essential parts of the employed biCMOS standard processes used for this purpose shall be briefly discussed.

The initial material used for the biCMOS standard process is a p silicon wafer having a specific electric resistance of, for example, 20 Ohm cm (Ω cm). After the implementation of a buried layer, a moderately highly doped n epitaxial layer having, for instance, a dopant concentration of 10^{15} cm^{-3}, with a thickness of approximately 1μm is deposited on the substrate. During the further processing, n and p wells (CMOS wells) will be implanted as regions into the n epitaxial layer. The n well simultaneously serves the purpose of generating the collector doping of the npn transistors. The dopant concentration of the n well is higher than that of the n epitaxial layer.

According to the present invention, the formation of the PIN photodiode may be performed in that a p^+ silicon wafer is used as initial or base material, wherein the wafer has formed thereon a p^- epitaxial layer with a thickness of approximately 15μm and a low dopant concentration of preferably substantially 10^{13} cm^{-3}. The standard n epitaxial layer following the implementation of the buried layer is deposited with a dopant concentration that is lowered to a range of approximately 10^{14} cm^{-3}. For both of these process modifications, no additional mask is necessary, since the biCMOS standard process includes the option of masking the n and p wells, as well as the buried layer with respect to the region of the photodiode.

In order to avoid a higher serial resistance of the PIN photodiode, not only the p well used for the lateral insulation of the PIN photodiode is used as an anode terminal, but also an additional backside contact of the bottom side of the substrate may be used, which may optionally, at least in this area, be thinned. It is sufficient, for example, to attach the thinned chip to a lead frame or a conductive area of a wiring board by means of a conductive adhesive.

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The present invention will be illustrated in more detail by means of schematic drawings and exemplary embodiments.

Figure 1 illustrates the structure of a PIN diode in one exemplary embodiment.

Table 1 depicts measurement results and a comparison.

Figure 2 illustrates, in a second exemplary embodiment, the structure of a PIN photodiode.

Figure 3 represents the progression of the electric field as is obtained with the conventional biCMOS standard process for the PIN diode region.

Figure 4 depicts the progression of the electric field as is obtained for the PIN diode region according to the structure of Figure 1 or Figure 2 (solid line) and for the case that the dopant concentration in the n epitaxial layer 9 is not reduced to an amount of substantially 10^{14} cm^{-3} to 10^{15} cm^{-3} (dashed line). This indicates that the p^- epitaxial 10 layer alone would not resolve the problem.

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Table 1 includes the measurement results of photodiodes implemented by a non-modified and a modified biCMOS process, respectively. It is evident that according to the modification of the present invention for a wavelength of 670 nm, an integrated photodiode having a quantum efficiency of more than 95% may be obtainrd, wherein the short rise and fall times allow a processing bit rate of up to 1 Gbit/second. A reduced junction capacity C_D allows for an increased photodiode area, which represents a further advantage.

Figure 1 illustrates the exemplary embodiment according to claims 16 to 21, while considering the discussion associated therewith provided on pages 2 and 3.

Existing layers and structures will be discussed in more detail with reference to a further illustrative embodiment according to Figure 2. Figure 2 represents a vertical structure of

a PIN photodiode. The intrinsic i-zone is formed by two slightly doped epitaxially grown layers 9, 10. The layer following the substrate 11, is a p-type layer. The further following layer is an n-type layer. To obtain such a structure, a standard biCMOS process with respective modifications is used.

Typically, for the standard process a base material is used starting from a p-type wafer having a specific resistance of approximately 20 Ω cm. Instead of this wafer type, here a modified, but, nevertheless, commercially available, wafer is used having an epitaxially deposited slightly doped p layer with a thickness of, for example 15μm, wherein the dopant concentration may, for example, be $10^{13}\,cm^{-3}$. This is the layer 10.

According to the standard process, after the implementation of buried layers 23, 22 a moderately highly doped n layer is formed on the substrate, which may have a thickness of, for example, 1μm. This epitaxial layer 9 may be doped within a range of $10^{15}\,cm^{-3}$. During the further processing, n-type and p-type wells are implanted in the same way as in the biCMOS process.

The n-zone 25 (the n^+ region) simultaneously serves the purpose of generating the collector doping and provides for the contact or terminal of a cathode K. The doping of the p wells extends into the n layer 9 and into the buried layers 23, 22. The p wells 20, 21 have formed therein p doping zones for receiving the anodes A1, A2.

On the top surface of the silicon wafer accordingly processed, wherein the top surface is denoted as top face or light side 30, the anodes A1, A2 and the cathode, as well as the light receiving collector zone 25 (in the form of an n^+ region) are provided. This top surface may be provided in a substantially even or planar form.

Oppositely arranged to the top side is provided a bottom side or back side 31 which follows the substrate 11. This back side is also provided with an anode A3, which may be formed as an area anode or as a locally restricted anode. This anode is denoted as a back side anode and forms an anode contact area of the PIN diode at the back side 31, wherein this anode is additional to the anodes A1 and A2 at the light side (top surface). The epitaxial layer 9 is delineated at its edges (laterally) by p regions 20, 21, which are shown in a vertical section.

Structurally, the area of the back side anode may be located higher or deeper, which may be achieved by a thinning or reduction of the thickness of the silicon wafer, which is not illustrated in the drawings.

The formation of the contacts is preferably performed from top side 30 with respect to all of the illustrated anodes A1, A2 and A3.

Trench contacts may be provided so as to form one or more anode terminals or contacts by these trench contacts, in particular, moderately deep contacts. These trenches are not explicitly shown.

The meaning of the notions "highly doped" or "slightly doped", with respect to the grown epitaxial layer 9, is a dopant concentration of approximately 10^{14} cm^{-3}. The dopant concentration of the first epitaxial layer 10, which is formed on the substrate 11 or which is already present there, is preferably a low dopant concentration in the range of 10^{13} cm^{-3}.

If the dopant concentration of the upper most layer 9 is lowered, a fast PIN photodiode is obtained, represented by the short rise and fall times as shown in Table 1. The transistor may not "experience" a great deal of this reduction of the dopant concentration, that is, the transition time and the current gain factor are slightly or hardly changed.

The two modifications with respect to the standard manufacturing process of a biCMOS process reside in the fact that a p wafer having an epitaxially deposited p layer with a low dopant concentration is used as the initial material. This epitaxial layer is slightly doped. The second modification resides in that fact that the dopant concentration of the further epitaxial layer formed thereon, in this case the n layer 9, is also maintained at a low level. For both process modifications, no additional mask is required with respect to the standard process.

Thus, the manufacturing process is already described in full detail with respect to the standard biCMOS manufacturing sequences and the modifications associated therewith by means of the above-specified description. The manufacturing process, nevertheless, shall be summarized. For example, the photodiode of Figure 2 or a photodiode according to Figure 1 is formed on the basis of an initial material, which is represented by a p silicon wafer having an epitaxially grown layer 10 with a thickness of substantially 15μm at most. This layer has a dopant concentration as mentioned above, which may be referred to as a slight or low dopant concentration. Next, an n epitaxial layer 9, which is used in a standard fashion, is grown, Its dopant concentration is maintained at a low

level, in the range of approximately 10^{14} cm^{-3}. This growth process of the epitaxial layer 9 is preceded by the formation of the buried layers 22, 23.

Next, the n and p wells are incorporated so as to allow contact with the anodes. Furthermore, all further standard process steps of the specified technology are performed. Hereby, an n^+ region 25 is incorporated into the n^- epitaxial layer, wherein the region 25 serves for the contacting of the cathode. This region is denoted as 25 in Figure 2 and faces the light side and thus, represents the light receiving side or top side 30. Laterally, this region is delineated by a p region 20, 21, which is provided around the cathode region 25 within the epitaxial layer 9 and which extends vertically preferably down to the buried layers 23, 22.

In addition to the aforementioned anodes A1, A2, which are incorporated into the p wells, a further anode A3 is formed on the back side 31.

In one illustrative manufacturing process, after dicing, which is not shown, the present chips resulting from the previously-described method, a conductive adhesive may be deposited so as to attach these chips to a lead frame. The chips may also be attached to a conductive area of a wiring board so as to be electrically contacted thereto. This is done when a serial resistance of the chip is obtained which is not sufficient.

At the front side, a protective covering of the silicon wafer may be used during or prior to thinning of the backside 31, at least within the area of the PIN photodiode of the silicon crystal shown in Figure 2. The process of thinning may be accomplished by grinding or polishing.

A further alternative is to not specifically form the anode contact area (the backside anode A3) and, thus, to not electrically contact the same. Contacting of the anode, is therefore, performed via the anodes A1, A2 on the top side (light side).

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